

Verify any silicon.

Master Design Verification, Verilog, SystemVerilog, and UVM. Gain the exact skill sets required to secure placements at the world's top tech and semiconductor companies.

The Ecosystem



Visual & Structured Learning

Master complex concepts like UVM hierarchy and timing diagrams through interactive platforms, visual blocks, and flowcharts.



Cloud Simulator IDE

Write, compile, and debug instantly in your browser. We remove the friction of environment setup so you focus on design.



Assessment Tracking

Quantify your readiness. Take module-wise quizzes, track your analytics, and ensure you're interview-ready.

Why Train With Us?

100% Hands-On Focus

Deploy your knowledge immediately. Theory is followed by rigorous daily coding, treating the terminal as your primary environment.

Specialized for DV Roles

Unlike generic VLSI courses, we hyper-focus on Design Verification using SystemVerilog and UVM—the most lucrative skillset.

Industry Standard Protocols

Bridge the "fresher gap" by working on live projects implementing protocols like AXI, AHB, and APB.

TARGETING TOP GIANTS



6-Month Comprehensive DV Program

The ultimate transformation journey. Start with foundational digital gates and graduate by verifying complex industry-standard protocols using the Universal Verification Methodology (UVM).

Month 1: Digital Electronics & Verilog Fundamentals

Mastering the hardware mindset.

- Logic gates, K-Maps, Combinational & Sequential circuits.
- Verilog syntax, Data types, Operators, Gate-level, Dataflow, and Behavioral modeling.
- Daily hands-on coding assignments on basic blocks.

Month 2: Advanced Verilog & Mini Projects

Architecting complex digital structures.

- Advanced FSM design (Mealy/Moore variations).
- Memory modeling (RAM, ROM, Synchronous/Asynchronous FIFOs) robust Verilog testbenches.
- **Project:** RTL Design and testing of a parameterized Async FIFO.

Month 3: SystemVerilog Core & OOP Concepts

Transitioning to dynamic verification languages.

- Advanced Data Types (Queues, Associative Arrays).
- Object-Oriented Programming (Classes, Handles, Inheritance, Polymorphism, and Virtual methods.).
- Inter-Process Communication (Mailboxes, Events, Semaphores).

Month 4: SV Randomization, Coverage & Interfaces

Building a layered testbench.

- Constrained random generation (rand, randc, constraints blocks).
- Functional Coverage (Covergroups, Coverpoints, Bins).
- SystemVerilog Assertions (SVA) basics, Interfaces, Modports, Clocking blocks.

Month 5: UVM Architecture & Components

Adopting the industry standard methodology.

- UVM Class hierarchy and Factory overrides.
- UVM Phases (Build, Connect, Run, etc.) & TLM Ports and connection mechanics.
- Developing UVM Components (Driver, Monitor, Sequencer, Scoreboard).

Month 6: Live Protocol Projects & Placement Drive

Becoming interview-ready.

- **Major Project 1:** UVM Verification of AMBA APB Protocol.
- **Major Project 2:** UVM Verification of AMBA AHB/AXI (Subset).
- Resume building and optimization for ATS scanners.
- 1:1 Technical Mock Interviews with feedback, HR round preparation and placement assistance.

Start your journey today

Instant access to the power of SystemVerilog and UVM.

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Short-Term Specialized Tracks

Intensive, focused modules designed to upskill specific areas of your verification knowledge. Ideal for targeted revision or rapid portfolio building.

45-Day Specialized Tracks (Training and Certification programs)



Digital Electronics

Master logic gates, FSMs, and combinational/sequential circuits.

- K-Map Minimization
- Sequential Circuits (Flip-Flops)
- Setup/Hold Timing Analysis



Verilog HDL

Transition from logic to code. RTL modeling and robust testbenches.

- Blocking vs Non-Blocking
- Behavioral Modeling
- FSM Design & Coding



SystemVerilog

Deep dive into OOP concepts, randomization, and coverage.

- Inheritance & Polymorphism
- Constrained Randomization
- Functional Coverage



UVM Basics

Understand UVM class hierarchy, factory mechanics, and phases.

- Factory Mechanics & Overrides
- TLM Ports & Connectivity
- Building UVM Agents

Project Advancement Track

Bridge the gap between academia and industry by implementing real-world protocols.



Async FIFO



AMBA APB



Complex ALU

1-Week Verilog Masterclass

Rapid Revision Bootcamp

A high-intensity refresh of your core Verilog concepts designed for upcoming interviews.



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The Semiconductor Boom

Why VLSI is the most lucrative career path of the decade, and how Design Verification sits at the center of the hardware revolution.

Why Design Verification?



The AI & EV Revolution

The rise of Artificial Intelligence, 5G, and Electric Vehicles requires highly complex ASICs and SOCs, driving unprecedented demand for chip designers.



70% of Project Cycle

In modern chip manufacturing, approximately 70% of the effort and time is dedicated to Verification to prevent million-dollar silicon respins.



Premium Compensation

Due to the high stakes and critical nature of the role, DV Engineers command some of the highest entry-level packages in tech hubs like Bangalore.

The VLSI Career Roadmap

1

Foundational Digital Design

Understanding how gates, muxes, and flip-flops interact. This is the bedrock of understanding how hardware physically behaves.

2

Hardware Description (Verilog/VHDL)

Translating logic into code. Learning RTL design to build functional blocks like Adders, Counters, and State Machines.

3

Verification & OOP (SystemVerilog)

The shift from creating to breaking. Writing robust object-oriented code, randomized constraints, and coverage models to test RTL.

4

Industry Standard Methodology (UVM)

The pinnacle of verification. Building reusable, scalable verification environments used by every major semiconductor company worldwide.

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Launch Your Career: The Fresher's Guide

A strategic blueprint to stand out from the crowd and secure a Design Verification role at industry-leading companies right out of college.

Bridging the "Fresher Gap"

University curriculums teach theory, but companies hire for practical execution. Here is the exact checklist to prove to recruiters that you are project-ready.

1 Master the Niche

Don't be a generalist. Deeply understand SystemVerilog OOP constructs, constrained randomization, and UVM phasing. It's the #1 skill HR looks for in DV resumes.

2 Build Protocol Portfolios

Companies don't test basic gates; they test protocols. Implementing a verification environment for AMBA APB or AXI shows you understand how real system-on-chips communicate.

3 Showcase on GitHub & LinkedIn

Upload your testbenches, waveforms, and documentation to GitHub. Post your project block diagrams on LinkedIn to attract recruiters from top tier companies.

4 ATS-Optimized Resumes

Ensure your resume passes Applicant Tracking Systems by including exact keyword matches: "UVM," "Coverage-Driven Verification," "SVA," and "AMBA Protocols."

Stop Reading. Start Verifying.

At LogicSilicon, we provide the curriculum, the cloud IDE, the protocol projects, and the mentorship to get you placed.

[Enroll Today](#)

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Mentorship & Success

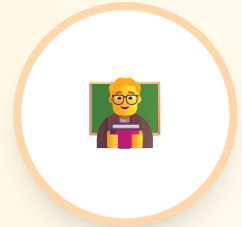
Hear from engineers who transformed their careers through our hands-on Design Verification training.

MENTOR HIGHLIGHT

Bridging the gap between theory and industry reality

With hands-on experience at industry leader **Synopsys**, Akash Bagwan provides 1:1 mentorship, rigorous mock interviews, roadmap planning, and detailed project debugging to ensure you are project-ready for top-tier roles.

1:1 Dedicated Mentorship Available



Student Success Stories

PN

"The 5-day digital logic revision at the start was exactly what I needed to refresh my basics. From there, transitioning into Verilog felt seamless. Implementing the Async FIFO project on their cloud IDE was the highlight of this internship!"

— Piyush Nagle, B.Tech Student

VP

"LogicSilicon's integrated ecosystem is brilliant. Using the LMS for theory, coding directly on the IDE, and testing my knowledge on the assessment portal made learning Verilog highly efficient. The final FIFO project was incredibly rewarding."

— Vinayak Patidar, B.Tech Student

KJ

"This training bridged the massive gap between my B.Tech syllabus and actual industry work. Writing testbenches for the Async FIFO gave me hands-on experience that I could never have gotten from just reading textbooks."

— Khwahish Joshi, B.Tech Student

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